WHAT IS CLAIMED IS:

1. A circuit comprising:

a compression circuit coupled to receive data values and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

2. The circuit of claim 1 wherein:

the compression circuit is coupled to receive the data values from a plurality of cells in a memory device and is structured to generate first and second compressed data signals based on the data values, the first and second compressed data signals being equal to the data values if the data values are all the same and the first and second compressed data signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second compressed data signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first compressed data signal during a leading edge of the clock signal and to produce the second compressed data signal during a trailing edge of the clock signal within each cycle of the clock signal.

3. The circuit of claim 2 wherein the compression circuit comprises:

a plurality of pull-up transistors coupled to intermediate nodes and structured to bring the intermediate nodes to a high voltage;

a plurality of pull-down transistors coupled between data latches structured to latch the data values and the intermediate nodes, the pull-down transistors being structured to generate intermediate signals at the intermediate nodes based on the data values; and

a logic circuit coupled between the intermediate nodes and the double data rate circuit, the logic circuit being structured to generate the first and second compressed data signals based on the intermediate signals.

4. A circuit comprising:

a compression circuit having a plurality of inputs each coupled to receive a data signal and a plurality of compression outputs, the compression outputs being fewer than the inputs, the compression circuit being structured to generate a compressed data signal at each of the compression outputs based on the data signals; and

an output circuit coupled to the compression circuit and being structured to couple each compressed data signal to a single output on edges of a clock signal.

5. The circuit of claim 4 wherein:

the compression circuit is structured to generate first and second signals at first and second compression outputs based on the data signals, the first and second signals being equal to the data signals if the data signals are all the same and the first and second signals being different if the data signals are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first signal during a leading edge of the clock signal and to produce the second signal during a trailing edge of the clock signal within each cycle of the clock signal.

6. The circuit of claim 5, further comprising:

a plurality of latch circuits, each latch circuit having an input coupled to a read data path to receive a respective one of the data signals from a memory cell in a memory device and having a pair of inverters each having an output connected to an input of the

other inverter to hold the data signal, the latch circuits being coupled together to the compression circuit; and

the inputs of the compression circuit are coupled to the latch circuits to receive the data signals.

7. The circuit of claim 6 wherein the compression circuit comprises:

a plurality of pull-up transistors coupled to intermediate nodes and structured to bring the intermediate nodes to a high voltage;

a plurality of pull-down transistors coupled between the latch circuits and the intermediate nodes, the pull-down transistors being structured to generate intermediate signals at the intermediate nodes based on the data signals; and

a logic circuit coupled between the intermediate nodes and the double data rate circuit, the logic circuit being structured to generate the first and second signals based on the intermediate signals.

8. A memory device comprising:

a plurality of cells;

a compression circuit coupled to receive data values from the cells and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

9. The memory device of claim 8 wherein:

the compression circuit is structured to generate first and second compressed data signals based on the data values, the first and second compressed data signals being equal to the data values if the data values are all the same and the first and second compressed data signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second compressed data signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first compressed data signal during a leading edge of the clock signal and to produce the second compressed data signal during a trailing edge of the clock signal within each cycle of the clock signal.

10. The memory device of claim 9, further comprising:

addressing circuitry;

control lines;

address lines; and

data lines.

11. The memory device of claim 10 wherein the compression circuit comprises:

a plurality of data latches, each data latch having an input coupled to a read data path to receive a data value read from one of the cells and a pair of inverters coupled to receive the data value, each inverter having an output connected to an input of the other inverter to hold the data value;

a plurality of pull-up transistors coupled to intermediate nodes and structured to bring the intermediate nodes to a high voltage;

a plurality of pull-down transistors coupled between the data latches and the intermediate nodes, the pull-down transistors being structured to generate intermediate signals at the intermediate nodes based on the data values;

a logic circuit coupled between the intermediate nodes and the double data rate circuit, the logic circuit being structured to generate the first and second compressed data signals based on the intermediate signals.

12. A system comprising:

a processor;

a memory device having a plurality of cells; and

a test circuit comprising:

a compression circuit coupled to receive data values from the cells and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

13. The system of claim 12 wherein:

the compression circuit is structured to generate first and second signals at first and second compression outputs based on the data values, the first and second signals being equal to the data values if the data values are all the same and the first and second signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first signal during a leading edge of the clock signal and to produce the second signal during a trailing edge of the clock signal within each cycle of the clock signal.

14. The system of claim 13, further comprising:

an input/output device; and

a bus connected to the processor, the memory device, and the input/output device.

15. The system of claim 13, further comprising:

a test machine including the processor;

a write circuit;

a read and data compression circuit including the test circuit; and

wherein the test machine, the write circuit, the read and data compression circuit, and the memory device are connected together by communication lines.

16. A system comprising:

a processor; and

a memory device having a plurality of cells and being connected to the processor, the memory device having an internal test circuit comprising:

a compression circuit coupled to receive data values from the cells and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

17. The system of claim 16 wherein:

the compression circuit is structured to generate first and second signals at first and second compression outputs based on the data values, the first and second signals being equal to the data values if the data values are all the same and the first and second signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first signal during a leading edge of the clock signal and to produce the second signal during a trailing edge of the clock signal within each cycle of the clock signal.

18. The system of claim 17, further comprising:

a display unit;

an input/output device; and

a bus coupling the processor, the memory device, the display unit, and the input/output device.

19. The system of claim 18 wherein the system comprises a computer system, an information component, or an appliance.

20. A test system comprising:

a test machine;

a memory device having a plurality of cells and being coupled to the test machine to be tested; and

test circuitry comprising:

a compression circuit coupled to receive data signals from the cells and being structured to generate compressed data based on the data signals; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

21. The system of claim 20 wherein:

the compression circuit is structured to generate first and second signals at first and second compression outputs based on the data signals, the first and second signals being equal to the data signals if the data signals are all the same and the first and second signals being different if the data signals are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first signal during a leading edge of the clock signal and to produce the second signal during a trailing edge of the clock signal within each cycle of the clock signal.

22. The system of claim 21, further comprising a plurality of memory devices each having a plurality of cells, each of the memory devices being coupled to the test machine to be tested.

23. The system of claim 21 wherein the test circuitry is located in the memory device.

24. The system of claim 21 wherein the test circuitry is located in the test machine.

25. The system of claim 21 wherein the test circuitry is located between the test machine and the memory device.

26. A double data rate memory device comprising:

a plurality of cells;

a compression circuit coupled to receive data values from the cells and being structured to generate compressed data based on the data values; and

an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

27. The memory device of claim 26 wherein:

the compression circuit is structured to generate first and second compressed data signals based on the data values, the first and second compressed data signals being equal to the data values if the data values are all the same and the first and second compressed data signals being different if the data values are not the same; and

the output circuit comprises a double data rate circuit coupled to the compression circuit to receive the first and second compressed data signals and to a clock signal source to receive the clock signal, the double data rate circuit being structured to produce the first compressed data signal during a leading edge of the clock signal and to produce the second compressed data signal during a trailing edge of the clock signal within each cycle of the clock signal.

28. The memory device of claim 27, further comprising:

addressing circuitry;

control lines;

address lines;

data lines; and

a plurality of data latches, each data latch having an input coupled to a read data path to receive a data value read from one of the cells and a pair of inverters coupled to receive the data value, each inverter having an output connected to an input of the other inverter to hold the data value, the data latches being coupled together to the compression circuit.

29. The memory device of claim 28 wherein the compression circuit comprises:

a plurality of pull-up transistors coupled to intermediate nodes and structured to bring the intermediate nodes to a high voltage;

a plurality of pull-down transistors coupled between the data latches and the intermediate nodes, the pull-down transistors being structured to generate intermediate signals at the intermediate nodes based on the data values;

a logic circuit coupled between the intermediate nodes and the double data rate circuit, the logic circuit being structured to generate the first and second compressed data signals based on the intermediate signals.

30. A memory device comprising:

a plurality of memory cells;

means for compressing a plurality of data values read from selected ones of the memory cells into test data; and

means for producing the test data on edges of a clock signal.

31. A method for testing a memory device comprising:

writing data to cells in the memory device;

reading the cells to generate read data;

compressing the read data to generate test data; and

producing the test data at a single output on edges of a clock signal.

32. The method of claim 31 wherein:

compressing the read data comprises compressing the read data into two compressed data signals; and

producing the test data comprises alternately coupling the two compressed data signals to the single output on rising and falling edges of the clock signal.

33. The method of claim 32 wherein:

compressing the read data comprises generating first and second compressed data signals to be equal to the read data if all the read data are the same and generating the first and second compressed data signals to be different if all the read data are not the same; and

producing the test data comprises coupling the first and second compressed data signals to a double data rate circuit structured to couple the first compressed data signal to the single output on a rising edge of the clock signal and coupling the second compressed data signal to the single output on a falling edge of the clock signal.

34. The method of claim 33, further comprising analyzing the first and second compressed data signals at the single output to determine that the cells store data properly if the first and second compressed data signals are the same and to determine that the cells do not store data properly if the first and second compressed data signals are not the same.

35. A method for testing a plurality of memory devices comprising:

writing data to cells in each memory device;

reading the cells to generate read data;

compressing the read data from each memory device to generate test data; and

producing the test data for each memory device at a single output on edges of a clock signal.

36. The method of claim 35 wherein:

compressing the read data comprises compressing the read data into two compressed data signals for each memory device; and

producing the test data comprises alternately coupling the two compressed data signals to the single output for each memory device.

37. The method of claim 36 wherein:

compressing the read data comprises, for each memory device, generating first and second compressed data signals to be equal to the read data of the memory device if all the read data from the memory device are the same and generating the first and second compressed data signals to be different if all the read data from the memory device are not the same; and

producing the test data comprises coupling the first and second compressed data signals for each memory device to a double data rate circuit structured to couple the first compressed data signal to the single output on a rising edge of the clock signal and to couple the second compressed data signal to the single output on a falling edge of the clock signal.

38. A method for operating an integrated circuit test machine comprising:

writing a test data value to selected cells in each of a plurality of memory devices;

reading the selected cells to generate read data for each memory device;

compressing the read data for each memory device into test data;

producing the test data for each memory device at a single output on edges of a clock signal; and

analyzing the test data at each output to determine if the selected cells in each memory device have stored the test data value properly.

39. The method of claim 38 wherein:

compressing the read data comprises compressing the read data into two compression signals for each memory device; and

producing the test data comprises alternately coupling the two compression signals to the single output for each memory device.

40. The method of claim 39 wherein:

compressing the read data comprises, for each memory device, generating first and second compression signals to be equal to the read data if all the read data are the same and generating the first and second compression signals to be different if all the read data are not the same; and

producing the test data comprises coupling the first and second compression signals for each memory device to a double data rate circuit structured to couple the first compression signal to the single output on a rising edge of the clock signal and to couple the second compression signal to the single output on a falling edge of the clock signal.

41. The method of claim 40 wherein analyzing the test data comprises analyzing the first and second compression signals at each output to determine that the selected cells stored the test data value properly if the first and second compression signals are the same and to determine that the selected cells did not store the test data value properly if the first and second compression signals are not the same.

42. A method for testing a memory device comprising:

writing data to cells in the memory device;

reading the cells to generate read data;

a step for compressing the read data into test data; and

a step for producing the test data at a single output.

43. A method for testing a memory device comprising:

selecting a plurality of test cells from cells in the memory device;

writing a test data value to each of the selected cells;

reading each selected cell to generate a plurality of read data values;

latching the read data values;

compressing the read data values into two intermediate data values;

converting the intermediate data values into first and second compressed data values, the first and second compressed data values being equal to the read data values if the read data values are all the same, the first and second compressed data values being different if the read data values are not all the same;

generating a clock signal;

producing the first compressed data value at an output on a rising edge in a single period of the clock signal;

producing the second compressed data value at the output on a falling edge in the single period of the clock signal; and

analyzing the first and second compressed data values at the output to determine that the cells in the memory device stored the test data value properly if the first and second compressed data values are equal.

44. A method for testing a double data rate memory device comprising:

writing data to cells in the memory device;

reading the cells to generate read data;

compressing the read data to generate test data; and

producing the test data at an output of a double data rate circuit on edges of a clock signal.

45. The method of claim 44 wherein:

compressing the read data comprises generating first and second compressed data signals to be equal to the read data if all the read data are the same and generating the first and second compressed data signals to be different if all the read data are not the same; and

producing the test data comprises coupling the first compressed data signal to the output of the double data rate circuit on a rising edge of the clock signal and coupling the second compressed data signal to the output of the double data rate circuit on a falling edge of the clock signal.